IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the present application:

1-43. (Canceled)

44. (New) A processor comprising:

a plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor, the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

a RISC/CISC assembly code level, and

a free pipeline assembly code level.

45. (New) A processor as recited in claim 44, wherein the free pipeline assembly code level comprises a native machine language of the processor.

46. (New) A processor as recited in claim 44, wherein the plurality of hierarchical instruction levels further comprise a vector processing assembly code level.

47. (New) A processor as recited in claim 46, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers.

48. (New) A processor as recited in claim 44, wherein the plurality of functional units comprise a multiplier unit and an arithmetic logic unit (ALU), and wherein each of the

plurality of functional units has an output that can be explicitly referenced in instructions defined from the instruction set.

49. (New) A processor as recited in claim 48, further comprising:

a plurality of dedicated output buses, one for each of the functional units; and

a plurality of bus registers, each coupled to store the output of only a corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses.

50. (New) A processor as recited in claim 49, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units.

51. (New) A processor comprising:

a plurality of functional units, including a multiplier unit and an arithmetic logic unit, to execute operations defined from an instruction set of the processor, wherein each of the plurality of functional units has an output that can be explicitly referenced in instructions defined from the instruction set.

52. (New) A processor as recited in claim 51, further comprising:

a plurality of dedicated output buses, one for each of the functional units; and

a plurality of bus registers, each coupled to store the output of only a corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses.

53. (New) A processor as recited in claim 52, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units.

54. (New) A processor as recited in claim 51, wherein the instruction set has a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

a RISC/CISC assembly code level; and

a free pipeline assembly code level.

55. (New) A processor as recited in claim 54, wherein the free pipeline assembly code level comprises a native machine language of the processor.

56. (New) A processor as recited in claim 54, wherein the plurality of hierarchical instruction levels further include a vector processing assembly code level.

57. (New) A processor as recited in claim 56, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers.

58. (New) A processor comprising:

a multiplier unit adjustable to multiply integer data words of any of a plurality of different lengths in response to instructions defined in an instruction set of the processor, the plurality of different lengths being integer multiples of each other, wherein the instruction set has a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor;

an arithmetic logic unit (ALU) adjustable to perform arithmetic operations on integer data words of any of the plurality of different lengths in response to instructions defined in the instruction set;

a shift register to perform shift operations in response to instructions defined in the instruction set;

a plurality of dedicated output buses, one for each of the multiplier unit, the ALU, and the shift register; and

a plurality of bus registers, each coupled to an output of a separate corresponding one of the multiplier unit, the ALU, and the shift register and to a separate corresponding one of the plurality of dedicated output buses, the bus registers to hold outputs of the multiplier unit, the ALU, and the shift register, respectively, wherein the outputs of the multiplier unit, the ALU, and the shift register can be explicitly referenced by instructions defined from the instruction set.

59. (New) A processor as recited in claim 58, wherein the hierarchy of instruction levels includes:

a RISC/CISC assembly code level;

a free pipeline assembly code level; and

a vector processing assembly code level.

60. (New) A processor as recited in claim 59, wherein the free pipeline assembly code level comprises a native machine language of the processor.

61. (New) A processor as recited in claim 59, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers.

62. (New) A processor as recited in claim 58, wherein the ALU has at least three operand inputs, further comprising:

a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving a plurality of bits from the control register to execute the three port parametrised logic function.